REMARKS/ARGUMENTS

Claim Objections

In the current Office Action, at the top of page 2, Claims 12-14 were objected to for being in improper dependent form. Claim 12 has been canceled. Claim 13 is rewritten in independent form. Accordingly, Applicants respectfully request the Examiner to withdraw this objection.

Claims 1-17 were objected to for use of parenthesis. The parenthesis have been removed, although Applicants respectfully note that the Examiner has not provided any support in the law for requiring this change.

Applicants submit that these changes do not affect the scope of the claims. If the Examiner believes the scope has changed, the Examiner is requested to explicitly explain their reason for same.

Claim Rejections – 35 U.S.C. §101

Claims 13 and 14 were rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. The Examiner said that a "computer readable medium" could be defined as a carrier wave. See the bottom of page 2 of the current Office Action.

This rejection is respectfully traversed. Applicants respectfully submit that Claims 13 and 14 (as originally filed) recited the term "computer readable storage medium". The Examiner has not shown why the word "storage" is to be ignored in these claims. This is a **prima facie defect** in the rejection under §101. When the claim word "storage" is taken into account, these claims fall within the statutory class of "product".

Thus, reconsideration and withdrawal of this rejection is respectfully requested.

Claim 1 Rejection

Claim 1 was rejected under 35 U.S.C. §102 as being anticipated by US Patent 4,785,400 granted to Kojima. Accordingly, the Examiner has taken the position that each and every element in Claim 1 is fully disclosed by Kojima. This rejection is respectfully traversed for numerous reasons, as discussed below.

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The Examiner stated in paragraph 3 on page 3 of the current Office Action that Claim 1's preamble is fully disclosed by Kojima in column 7, lines 55-59 which are reproduced below for convenience:

> A transformation from a row number comprising a page number i and a slot number j to a corresponding storage address of the data for that row within the main storage is carried out in accordance with the sequence of steps in FIG. 7.

Note that the above-quoted text merely describes a transformation. Specifically, a row number is transformed into a storage address in main storage. Firstly, nothing in the above-quoted text discloses that rows in a table of a database are updated. Secondly, nothing in the above-quoted text discloses use of row-identifier and value pairs. Accordingly, Claim 1's preamble is not fully disclosed by Kojima.

The Examiner further stated in page 3 of the current Office Action that Claim 1's first limitation of "repeatedly finding, and storing in a structure ..." is fully disclosed by Kojima in column 3, lines 10-22 and column 4 lines 51-54 which are reproduced below for convenience:

Column 3, lines 10-22:

> part 109 of the program 103 refers to the codes stored in the control block 106 and processes the search command received by the interface part 104 according to the process sequence designated by the codes, to provide results of the processing to the application program 102 by way of the interface part 104.
>
> During the processing, data required for the processing, but not yet loaded, is loaded into a data buffer area 110 in the main storage 101 from a data page area 141 in a subsidiary storage 102, in such a manner that data elements are separately loaded by units of the data elements contained within a unit area called a data page and having a fixed area size. The data pages are ran-

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Column 4 lines 51-54:

be processed. The row number table includes the data page address (page number and slot pointer number) for a table to be processed. Based upon a table definition table, such as 1003 or 1005 in FIG. 12, and a corre-

The above-quoted text from Column 3 merely teaches that a search command is processed to provide results, and any data not yet loaded into a buffer area is loaded. Moreover, the above-quoted text from Column 4 at most indicates that a table (called "row number table") includes Kojima's row identifier (page number and slot pointer number).

Note that the column 3 text quoted above explicitly states "search command" which is singular and not plural. Accordingly, nothing in the above-quoted text from Column 3 or Column 4 discloses or suggests that a "group" of row identifiers are used "repeatedly" by Kojima to find corresponding page numbers, and that Kojima stores the page numbers that are thus found in a structure. Instead, Kojima explicitly states in the above-quoted text from Column 3 that his data elements are "separately" loaded. Hence this is a third distinction (in addition to the two distinctions noted above in reference to Claim 1's preamble).

Note further that Claim 1 requires storing several block-identifiers in a structure, wherein the block identifiers are of blocks that contain rows identified by row-identifiers in the "group" (described above; whose values are to be used to update rows). Claim 1's structure is nowhere disclosed or suggested in the above-cited Columns 3 and 4 from Kojima's patent. Therefore, this is a fourth distinction over Kojima's patent.

Moreover, Claim 1 has been amended to explicitly state that a single operation is thereafter performed, to store in a cache multiple blocks that are identified in the structure. Support for this amendment is found throughout the application, including for example, the following language in paragraph [0026] on page 9: "As noted above, in many embodiments this is a single disk access operation, and on completion of this operation buffer cache 140 contains the corresponding blocks BLOCK1...BLOCKm."

The Examiner's only citation against this second limitation of Claim 1 was the following text from column 6 lines 7-19, column 7 lines 34-43 and column 7, lines 11-25:

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instruction and the displacement field (A) of the instruction, to indicate the detected kind of vector instruction to the vector ALU **1709**, which is comprised of a pipelined ALU. The set-up circuit **1703** reads the vector length from a general register designated by the R_1 field **1609** of the instruction **1601** to send the vector length to the vector ALU **1709**. The set-up circuit **1703** reads out an operand descriptor address from a general register designated by the R_2 field **1610** of the instruction **1601**, reads out an operand descriptor **1606** based upon the read out operand descriptor address, and, based upon the contents of the read out operand descriptor, reads out vector descriptors. The first element address and an

(Data buffer area **110** and data buffer directory **401**)

When a data page **302** in a subsidiary storage **112** is to be processed by the relational data base managing program **103**, the data in the data page **302** is transferred to a data buffer area **110** within a main storage **101** before the processing.

The data buffer area **110** is divided into data buffer units as shown in FIG. **6**. Each data buffer unit has its own number, has the same size as the data page **302**, and stores a copy of the necessary data page **302**. In connec-

entries belonging to one row of a table. For example, in the case of a slot for the first row of the table **202** of FIG. **2B**, data "A, **316**" is stored in the slot. Each slot has its own slot number. Each data page **302** includes slot pointers **303** each indicating a starting address of a respective one of the slots **304** within the same data page **302**. The slot pointers are stored at an area starting from the start address of the data page and according to the order of the corresponding slot numbers.

As is clear from the structure of the data page, a storage location of a row within the subsidiary storage **112** (FIG. **1**) can be designated by a data page number i and a slot number j. Therefore, the combination **301** of the data page number i and the slot number j is called a row number.

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Nothing in this text from Kojima's columns 6 and 7 (cited by the Examiner) states that the a single operation is performed by Kojima to fetch multiple pages. Moreover, nothing states that a structure containing page identifiers is used by Kojima to fetch into a buffer the pages that are identified in the structure. Hence these are two additional distinctions (in addition to the two distinctions noted above in reference to Claim 1's preamble and the two distinctions noted above in reference to Claim 1's first limitation). Thus far, a total of six distinctions have been documented herein.

Finally, note that Claim 1 requires use of a corresponding value in the pairs to update the blocks that have been fetched. This limitation is nowhere disclosed or suggested in the following text by Kojima that is cited by the Examiner(at the top of page 4 of the current Office Action):

> **main storage 101 thereby. The operand vector elements accessed by the address generator 1705 are sent to the vector ALU 1709 successivly and the resultant vector elements are successively sent from the vector ALU 1709 for example to the main storage 101. The operation by the vector ALU 1709 is continued until all elements designated by the vector length have been operated on. As the operation by the vector ALU 1709 and access to the main storage 101 are repeated by a pitch of one machine cycle, the total operation finishes very quickly.**

At most the above-quoted text may suggest that some operation is performed on Kojima's elements which are designated by vector length, but nothing states that the elements are identified based on "pairs" and that the values being updated are from the "pairs." Therefore, this is a seventh distinction of Claim 1 over Kojima's patent.

Thus, Applicants respectfully submit that Claim 1 is not anticipated by Kojima. Reconsideration and withdrawal of this rejection is respectfully requested. Claims 2-11 depend from Claim 1 and are, therefore, likewise patentable.

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Note that the above-presented arguments render moot the Examiner's rejections of one or more of the dependent claims as being obvious over the teachings of Kojima in view of one or more of Tolkin and/or Vagnozzi and/r Hashimoto. Applicants also hereby

traverse the Examiner's combination of these references as being unsupported by the prior art.

Claims 13-17 recite one or more limitations that are supported by arguments for patentability that are similar one or more of the arguments presented above in reference to Claim 1. Accordingly, these claims are also similarly patentable.

For the above reasons, Applicants respectfully request allowance of all pending claims. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 982-8203.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office to the fax number 571-273-8300 on October 25, 2006.

S. Omkar — Oct 25, 2006

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Respectfully submitted,

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